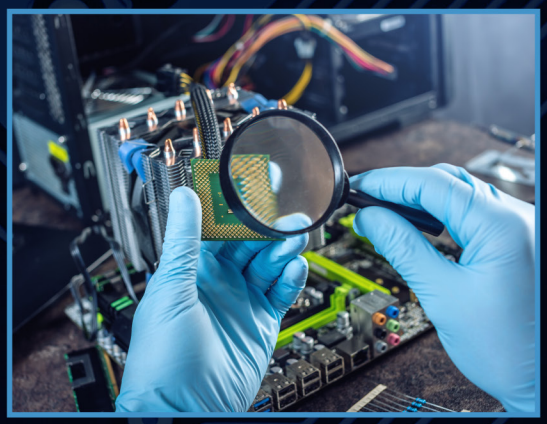
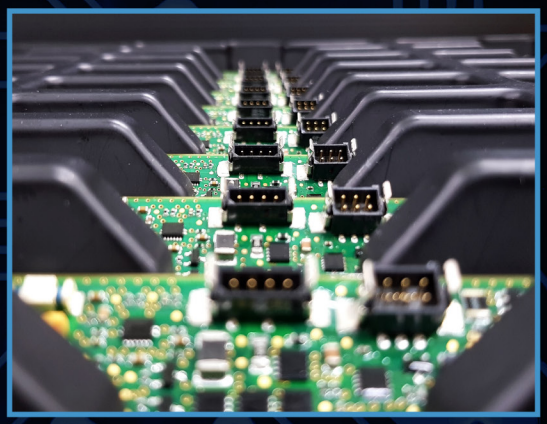
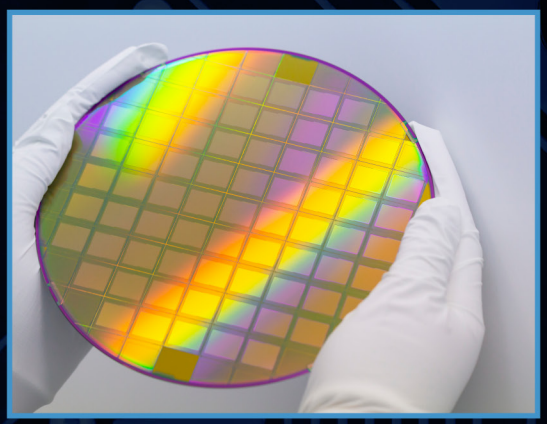






Strategic Opportunities for U.S. Semiconductor Manufacturing

Facilitating U.S. Leadership and Competitiveness through Advancements in Measurements and Standards

August 2022

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

The programs authorized by the Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act provide a historic opportunity to expand our domestic manufacturing capacity, help grow the research and innovation ecosystem for microelectronics and semiconductors in the U.S., and restore U.S. leadership in semiconductor manufacturing. The Department of Commerce and NIST are fully committed to ensuring the successful implementation of these programs.

Successful implementation of the CHIPS Act programs will require close coordination and input from industry and key stakeholders. As an important first step to engage industry and critical stakeholders, NIST sponsored a series of Semiconductor Metrology Workshops in April 2022 seeking input on how NIST can help address key measurement challenges facing the semiconductor industry. These workshops brought together over 800 attendees from industry, academia, and government. This report provides a summary of your input from the workshops on key measurement challenges facing the semiconductor ecosystem, strategies for addressing those challenges, and key areas where NIST can help.

As we heard from you, metrology challenges impacting the U.S. semiconductor industry are at a critical stage and urgently need to be addressed. The strategic opportunities outlined in this report will enable us to provide critically needed measurement services, advanced metrology R&D testbeds, innovative manufacturing metrologies, novel assurance and provenance technologies, and standards, and build even stronger partnerships with industry.

I want to thank you for your input and participation, and I look forward to continued engagement as we begin to build out and implement the metrology and standards programs to address the key strategic challenges outlined in the report.

Sincerely,

Laurie E. Locascio, Ph.D.
Under Secretary of Commerce for Standards and Technology &
Director, National Institute of Standards and Technology

NIST | NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Executive Summary

NIST | NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Semiconductors are critical to our Nation's economic growth, national security, and public health and safety. Revolutionary advances in microelectronics continue to drive innovations in communications, information technology, health care, military systems, transportation, energy, and infrastructure. The potential for microelectronics to create transformational change is growing exponentially as they become smaller, faster, and more sophisticated—delivering unprecedented performance. Next-generation systems, devices, and related technologies are critical to addressing society's most urgent needs.

The nation that leads in microelectronics research, development, and manufacturing will lead in defining and reaping the benefits from dynamic shifts in technology.

The ability to cost-effectively manufacture complex next-generation microelectronics devices and integrate them in novel systems and packages is a growing challenge, compounded by ever-greater requirements for performance, functionality, and security.

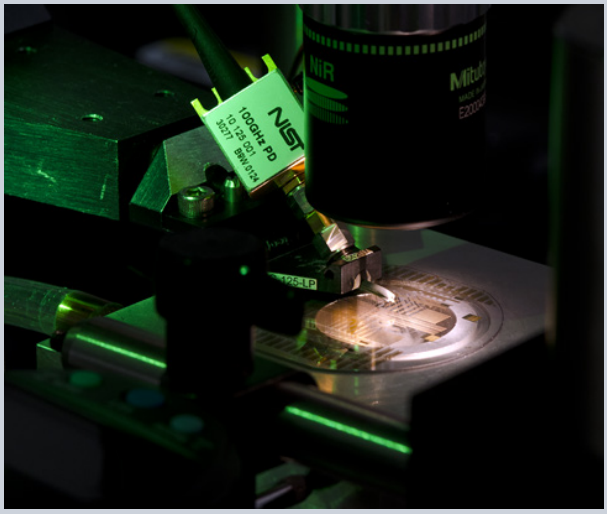
To strengthen the U.S. position in semiconductors, Congress authorized a set of programs known as the Creating Helpful Incentives to Produce Semiconductors for America Act (CHIPS Act) as part of the William M. (Mac) Thornberry National Defense Authorization Act (NDAA) for Fiscal Year 2021 (Pub. L. No. 116-283). These programs would help restore U.S. leadership in microelectronics manufacturing and ensure America's supply of leading-edge products by providing incentives and encouraging investment to expand production capacity and grow the innovation ecosystem for microelectronics research and development (R&D).

Leveraging decades of experience in next-generation devices, systems, and related technologies, NIST has a specific role authorized under the CHIPS Act to undertake critical metrology R&D that will strengthen the domestic semiconductor industry.

A key CHIPS Act priority is metrology research at the National Institute of Standards and Technology; specifically, the statute calls for NIST to ***"carry out a microelectronics research program to enable advances and breakthroughs….that will accelerate the underlying R&D for metrology of next-generation microelectronics and ensure the competitiveness and leadership of the United States…."***

Microelectronics in this report refers to integrated electronic devices and systems generally manufactured using semiconductor-based materials and related processing (i.e., in a semiconductor fabrication manufacturing facility, or "fab").

Such devices and systems include analog and digital electronics, power electronics, optics and photonics, and micromechanics, for memory, processing, sensing, and communications.



A photodiode pulse generator connected to a wafer probe to measure electrical pulses up to 110 GHz. This tool is used to calibrate oscilloscopes, vector signal analyzers, arbitrary waveform generators, large signal network analyzers, and light wave component analyzers. Many manufacturers of high-speed measurement equipment have purchased photodiode calibrations from NIST.

Photo Courtesy of Curt Suplee, NIST

Metrology challenges impacting the U.S. semiconductor industry are at a critical stage and urgently need to be addressed.

Metrology, the science of measurement and its applications, plays a key role in up to 50 percent of semiconductor manufacturing steps to ensure quality, yield, and performance. As devices become more complex, the ability to measure, monitor, predict, and ensure quality in manufacturing becomes much more difficult. For example, modern chips may contain over 100 billion complex nanodevices that are less than 50 atoms across—all must work nearly identically for the chip to function. Today, the domestic semiconductor industry faces these metrology challenges using workarounds and insufficient tools. The results are reduced in quality and manufacturing yields, increased costs for manufacturing, and slower product innovation.

Addressing metrology grand challenges will support increased production, innovation, and competitiveness in the domestic semiconductor industry.

Recognizing that metrology is critical to enabling future microelectronics innovation, NIST has worked with stakeholders to identify the critical challenges requiring R&D. Information gained by NIST through a series of workshops, a request for information, and discussions with major companies has informed a proposed strategic path forward focused on seven Grand Challenges.

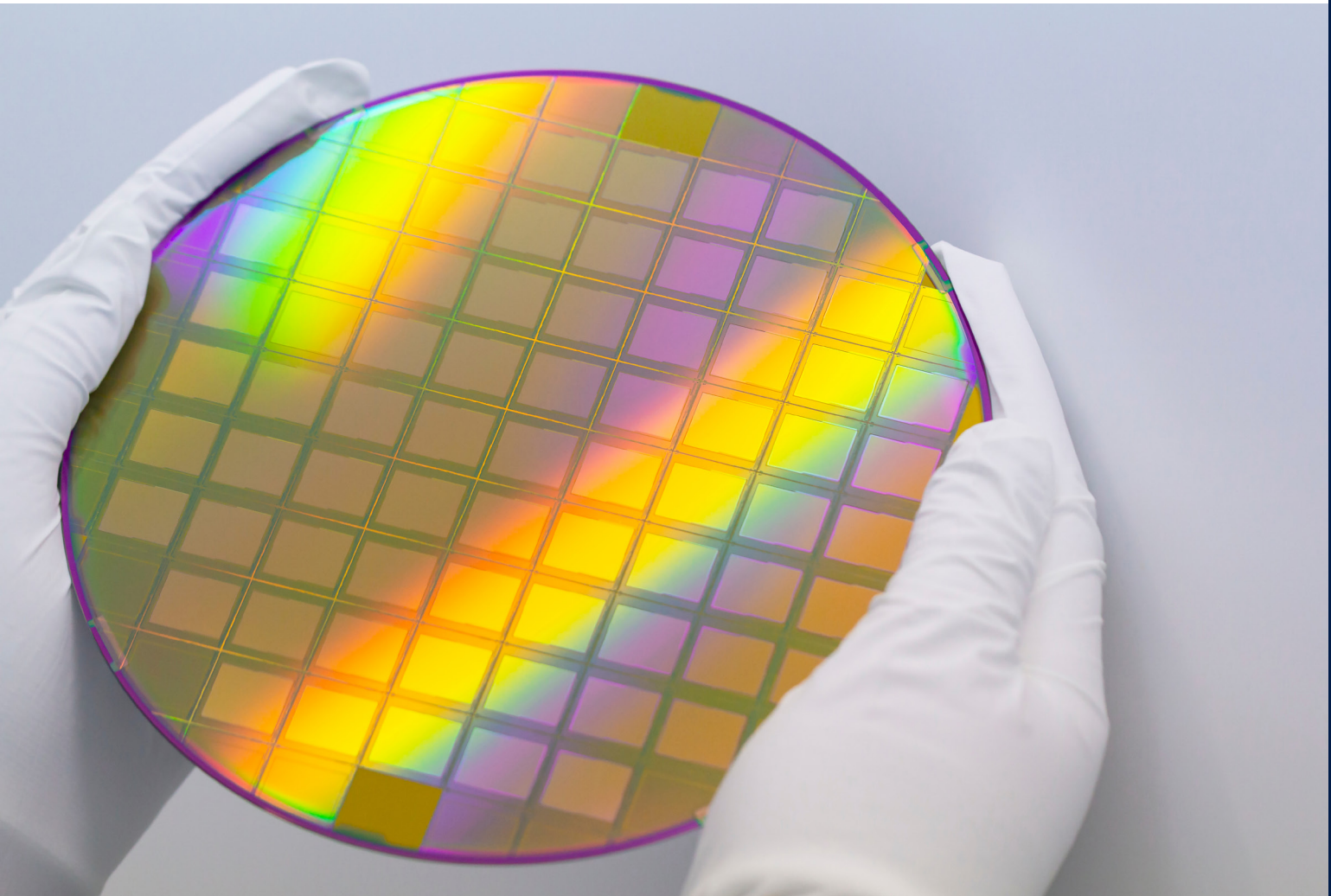
The Grand Challenges outline metrology R&D needed to strengthen the domestic semiconductor industry. Metrology is needed at all stages of semiconductor technology development, from basic and applied R&D in the laboratory to demonstrating proof of concept, prototyping at scale, factory fabrication, assembly and packaging, and performance verification prior to final deployment.

This report is a call to action.

Metrology underpins our ability to address the challenges faced by semiconductor manufacturers. Making investments in metrology capabilities today will future-proof technology needs and support U.S. leadership for the next generation of microelectronics.

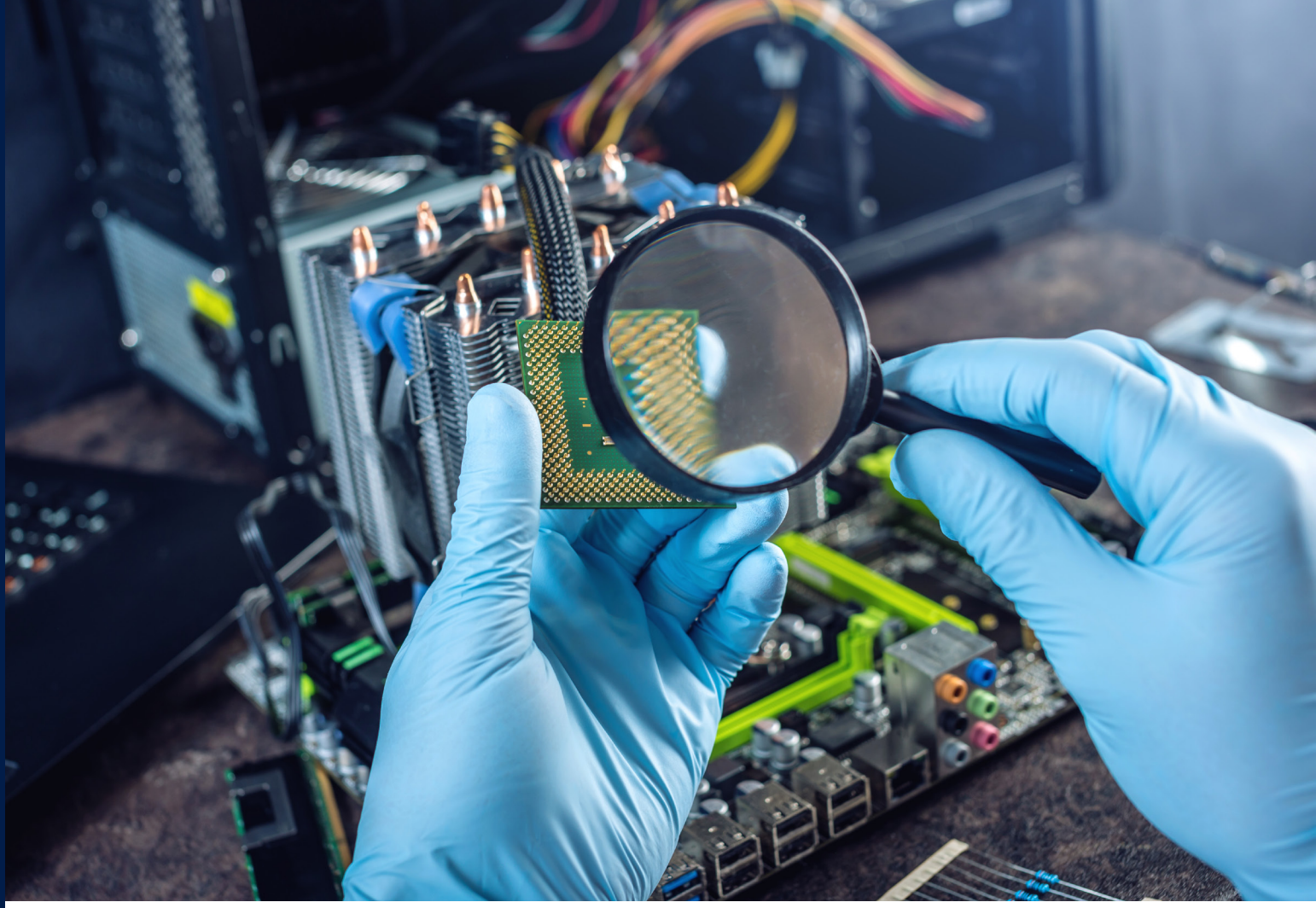
There is not a moment to lose in accelerating R&D on urgently needed metrology advances—and many high-impact outcomes to be gained, specifically by:

- *Advancing **U.S. leadership in documentary standards development** to strengthen U.S. global competitiveness in advanced microelectronics materials, design, manufacturing, and packaging.*
- *Developing and deploying **critically needed measurement services** (reference materials, reference data, calibrations) to drive U.S. leadership in microelectronics manufacturing and related technologies.*
- *Developing and deploying **innovative manufacturing metrologies** to enable U.S. industry to increase manufacturing yield, improve performance, and accelerate time to market for next-generation microelectronics.*
- *Developing and deploying **novel assurance and provenance technologies** to reduce microelectronics security risks across supply chains, from design and development to manufacturing, packaging, and end-of-life.*
- *Establishing **advanced metrology R&D testbeds** with state-of-the-art equipment and tools to drive measurement science innovations for next-generation microelectronics.*
- *Building and sustaining **collaborative partnerships with industry** to accelerate the transfer of technology from the laboratory to the commercial marketplace and support talent development and deployment.*



	GRAND CHALLENGE	STRATEGY
Metrology for Materials Purity, Properties, and Provenance	Meet increasingly stringent requirements for semiconductor materials purity, physical properties, and provenance across a diverse supply chain through development of new measurements and standards.	Develop measurement technologies, properties data, and standards focused on defect and contaminant identification to support uniform materials quality and traceability across the supply chain.
Advanced Metrology for Future Microelectronics Manufacturing	Ensure critical metrology advances keep pace with cutting-edge and future microelectronics and semiconductor manufacturing, while maintaining a competitive U.S. advantage.	Advance the physical and computational metrology tools adaptable to next-generation manufacturing of advanced complex, integrated technologies and systems.
Enabling Metrology for Integrating Components in Advanced Packaging	Provide enabling metrology spanning multiple length scales and physical properties for acceleration of advanced packaging for future-generation microelectronics.	Develop metrology for complex integration of sophisticated components and new materials to support a strong domestic advanced microelectronics packaging industry.
Modeling and Simulating Semiconductor Materials, Designs, and Components	Improve tools needed to effectively model and simulate future semiconductor materials, processes, devices, circuits, and microelectronic system designs.	Create advanced design simulators using multi-physics models and next-generation concepts such as artificial intelligence and digital twins, empowering U.S. microelectronics designers.
Modeling and Simulating Semiconductor Manufacturing Processes	Seamlessly model and simulate the entire semiconductor manufacturing process, from materials inputs to chip fabrication, system assembly, and end products.	Develop advanced computational models, methods, data, standards, automation, and tools to enable domestic semiconductor manufacturers to improve yields, accelerate time to market, and enhance competitiveness.
Standardizing New Materials, Processes, and Equipment for Microelectronics	Standardize the methods that will support and accelerate the development and manufacturing of microelectronics and advanced information and communications technologies.	Create standards, validation tools, and protocols for next-generation materials, processes, and equipment, paving the way for accelerated innovation and cost-competitiveness in U.S. industry.
Metrology to Enhance Security and Provenance of Microelectronic based Components and Products	Create the metrology advances needed to enhance the security and provenance of microelectronic components and products across supply chains and increase trust and assurance.	Pursue a comprehensive approach to hardware security protection that includes standards, protocols, formal testing processes, and advanced computational technologies while providing avenues for assurance and provenance of microelectronic components across the supply chain and end products.

TABLE OF CONTENTS



Foreword

This report was developed with input from renowned experts in the field of microelectronics through a series of NIST-hosted workshops, a request for information, and other sources. Major U.S. companies also provided their unique insights on this important topic.

This document provides a high-level perspective of the metrology challenges facing the U.S. semiconductor manufacturing industry and the associated strategic research and development (R&D) that is needed.

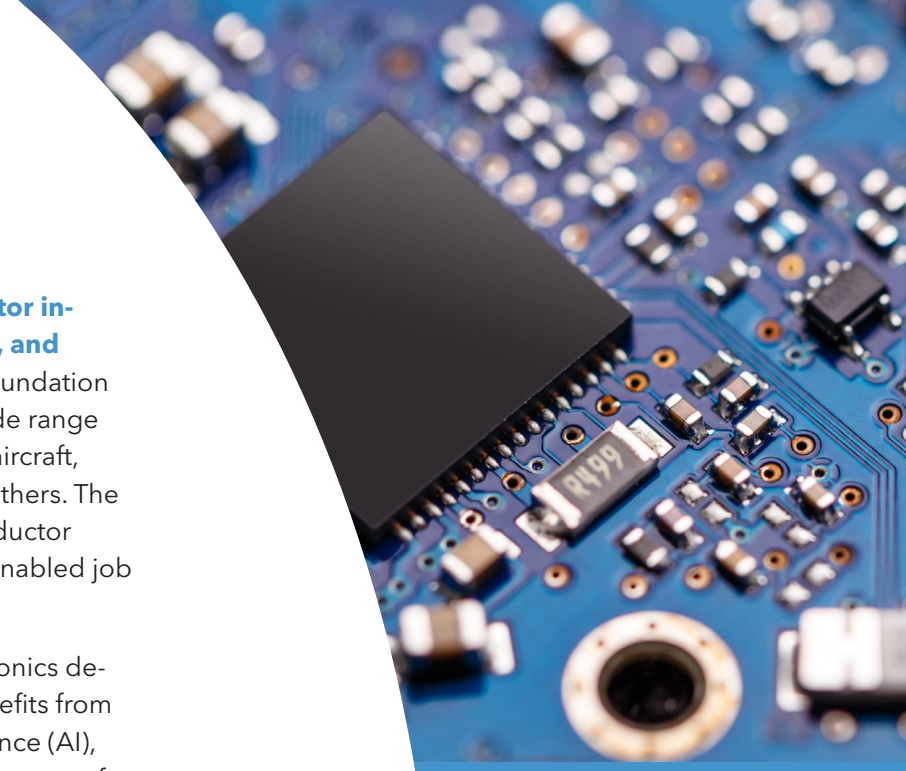
The report will be used by both public and private stakeholders to inform decisions about the metrology R&D and standards that should be pursued to transform and strengthen domestic semiconductor manufacturing.

Disclaimer

The views and opinions expressed herein do not necessarily state or reflect those of NIST or the United States Government. Certain commercial entities, equipment, or materials may be identified in this document to illustrate a point or concept adequately. Such identification is not intended to imply recommendation or endorsement by NIST, nor is it intended to imply that the entities, materials, or equipment are necessarily the best available for the purpose.

Official contribution of the National Institute of Standards and Technology; not subject to copyright in the United States.

Introduction



Advances in microelectronics by the semiconductor industry underpin U.S. economic strength, security, and technological standing. Semiconductors are the foundation of modern technologies and are embedded in a wide range of products, from communications to automobiles, aircraft, computers, medical devices, security systems, and others. The innovations made possible by advances in semiconductor technology have expanded the Nation's economy, enabled job growth, and transformed our way of life.

Moving forward, the nation that leads in microelectronics development will lead in defining and reaping the benefits from the industries of the future, such as artificial intelligence (AI), autonomous vehicles, advanced communications, internet of things, quantum computing, and many more.

The future of the chip industry is going to be made in America.

President Joe Biden, August 9, 2022

For over 50 years, reducing the size of transistors has allowed engineers to make circuits that are more complex and higher-performing, require less power, and are cheaper to produce. As geometric scaling reaches its practical limits, material-driven innovations at the nanoscale have become essential to the development of advanced devices. Today, complex integration of electronic and photonic technologies with the highly sophisticated CMOS (complementary metal–oxide–semiconductor) platform found in many computer microchips has emerged as a key driver and differentiator of performance and global competitiveness. Ultimately, ever-greater device- and system-level innovations will be needed as performance requirements continue to evolve along with modern technologies.

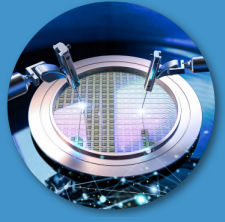
The ability to cost-effectively manufacture and test complex microelectronics devices at the nanoscale is a growing challenge, requiring concomitant advances in design, processing, and integration to ensure quality and performance. These systems are growing in complexity even as their components are shrinking in size. Increasingly, precision of materials, dimensions, and placement is integral to system performance, reliability, security, and safety. Metrology, the science of measurement and its applications, underpins our ability to address these challenges.

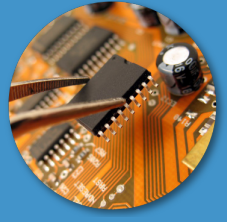
THE LANGUAGE OF MICROELECTRONICS

Front End semiconductor manufacturing is the first step in wafer manufacturing, where wafer-based devices like transistors, poly capacitors, non-metal resistors, and diodes are formed.

Back End refers to the last step of the manufacturing, where the wafer is cut, assembled, and placed into various packages.

The convergence of Front End and Back End for improved performance places unprecedented demand for rapid innovation in measurements and standards.





"We will see increased complexity in many advanced packaging options now and in the future—**there is an urgent need for advancements in metrology for all options.**"

E. Jan Vardaman, President, TechSearch International, NIST Semiconductor Manufacturing Metrology R&D Workshop, April 2022

WHAT IS METROLOGY?

Metrology is the science of measurement and its application. At NIST, work in metrology focuses on advancing measurement science and related standards to enhance economic security and improve quality of life.

Physical metrology—measurements of dimensional and physical properties for materials, devices, systems, and processes.

Computational metrology—physics-based modeling, reconstruction, and visualization of multi-dimensional information combined with physical metrology to analyze, predict, and control the performance of systems and processes.

Virtualization and automation—data collection, management, processing, and analytics combined with machine learning (ML), and other information for manufacturing process control, security, and authentication.

Measurement services—calibrations of machines and equipment, Standard Reference Materials (SRMs), standard reference data (SRD), and standard reference instruments (SRIs) to ensure traceability of manufacturing data to an established benchmark, i.e., the International System of Units (SI).

Measurement and documentary standards—specify definitions, dimensions, materials, processes, practices, performance, products, systems, services, test methods and sampling procedures, or classifications of components.

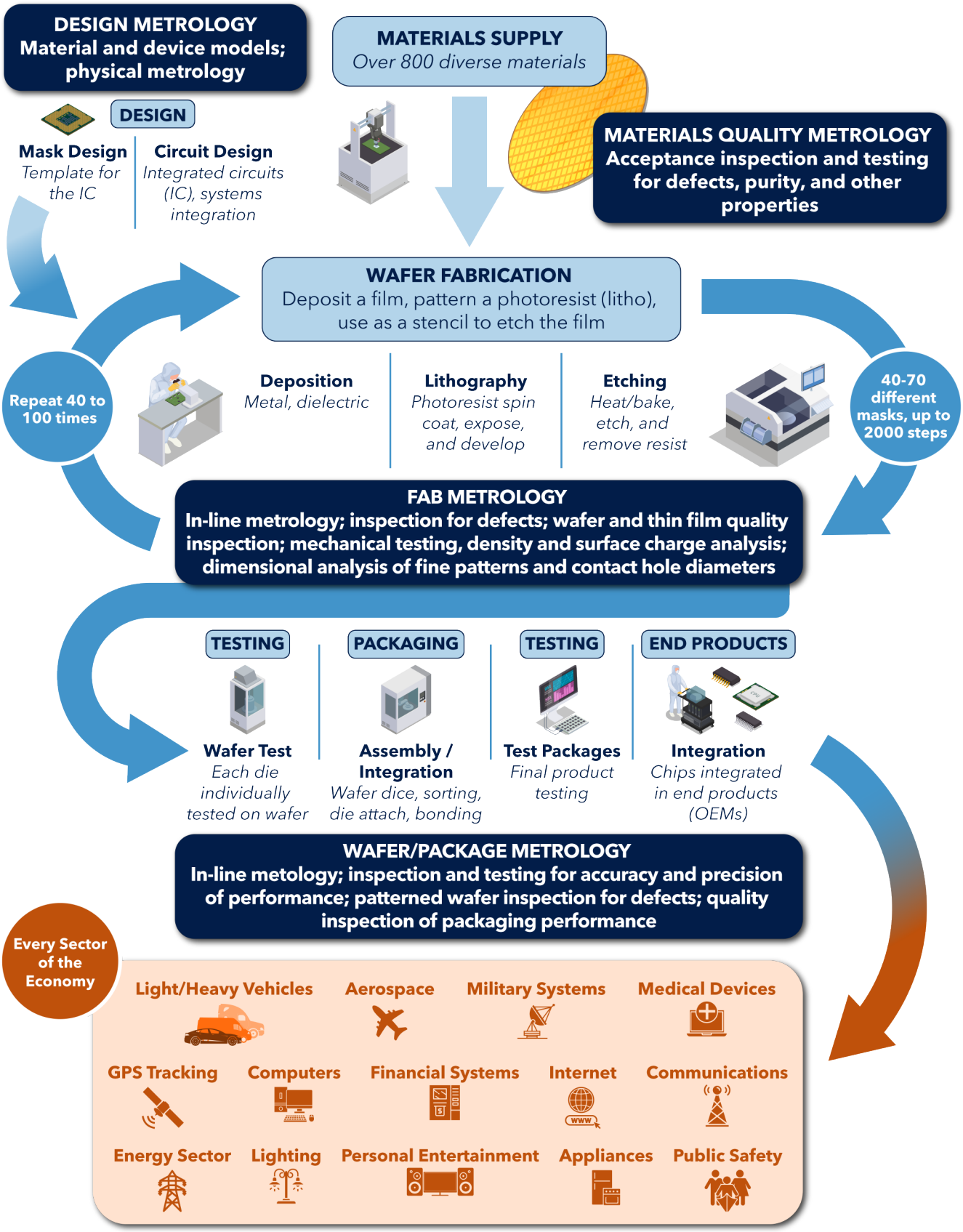
The Role of Metrology

Metrology research and development (R&D) is fundamental to all aspects of the semiconductor supply chain. In some cases, over 50 percent of semiconductor manufacturing involves measurement to ensure quality, yield, and performance. The importance of metrology increases as devices become smaller and more highly integrated and operate at higher frequencies or data rates. Today's semiconductors can have tens of billions of transistors on a square-centimeter-sized chip, all working together to meet specifications, requiring measurements of structure and composition at the atomic scale.

Through its leadership in standards and measurement science, the National Institute of Standards and Technology (NIST) has been a crucial partner in helping the U.S. microelectronics industry in the the development and manufacturing of next-generation devices. The companies that supply equipment, design, and materials to major semiconductor producers are largely U.S.-based and also critical to technology development.

Breakthroughs in measurement science, standards, material characterization, instrumentation, testing, and manufacturing capabilities are necessary to realize the potential of emerging 3D devices and 3D heterogeneous integration. As devices become more complex, highly integrated, and smaller, ensuring performance becomes more challenging. Meeting dimensional tolerances, performance, and reliability over a range of environments becomes increasingly difficult.

The needs encompass a broad spectrum of technology maturity from pilot scale prototyping and validation to production and commercialization, bridging work in the laboratory and the manufacturing plant.



Metrology has a significant impact on the semiconductor ecosystem, consuming a large portion of steps in chip manufacturing (50% and growing). As many as 30% of tools in fabrication are metrology/defects toolsets.

THE CHIPS ACT

Creating Helpful Incentives to Produce Semiconductors for America Act (CHIPS Act), part of the William M. (Mac) Thornberry National Defense Authorization Act (NDAA) for Fiscal Year 2021 (Pub. L. No. 116-283).

CHIPS Act Section *9906(e)*:

"MICROELECTRONICS RESEARCH AT THE NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY. *The Director of the National Institute of Standards and Technology shall carry out a microelectronics research program to enable advances and breakthroughs in measurement science, standards, material characterization, instrumentation, testing, and manufacturing capabilities that will accelerate the underlying research and development for metrology of next-generation microelectronics and ensure the competitiveness and leadership of the United States within this sector.*"

A Call to Action

Future applications of microelectronics will be transformative. Next-generation devices will enable extraordinary gains in advanced communications, intelligent systems, and high-speed computing that are hard to imagine today. U.S. competitiveness in this critical field is fundamental to the Nation's long-term economic growth, national defense, health, and safety.

While the U.S. once led the world in semiconductor manufacture, it now accounts for about 12 percent of global production and produces none of the most advanced chips. Countries around the world are investing in semiconductors, with China striving to become a global leader. All nations will depend heavily on information and computing technologies fueled by semiconductors.

The U.S. government has enacted authorizing legislation and appropriated funds to strengthen America's semiconductor industry and supply chains and spur robust investments in innovation. The CHIPS Act lays out a number of goals: to protect and extend U.S. semiconductor technology leadership, ensure a secured supply of chips for critical sectors, and promote the long-term economic viability of this important U.S. industry. Programs under the CHIPS Act would expand manufacturing capacity for both advanced and mature microelectronics technologies. They would also help grow the research and innovation ecosystem for microelectronics and semiconductor research and development R&D in the U.S.

This report outlines a set of strategic grand challenges for metrology and related R&D that is necessary to enable innovation and bolster competitiveness in the domestic semiconductor industry. NIST has a specific role authorized under the CHIPS Act to undertake this essential metrology R&D, which is part of the foundation for leading innovations and advances in domestic microelectronics.

Metrology is foundational to semiconductor manufacturing. Making investments in metrology capabilities now will future-proof our technology needs and ensure that domestic producers are cost-competitive in driving the rapid evolution of microelectronics.

The opportunity is now. There is not a moment to lose in accelerating R&D on critically needed metrology—enabling advances and breakthroughs and supporting our Nation's leadership in next-generation microelectronics.

Strategic Opportunities for Semiconductor Manufacturing

"The greatest risk is not investing in semiconductor R&D for our future…. **Metrology advances** are needed to reduce cycle time, obtain insight, and push the frontier."

Todd Younkin, President and Chief Executive Officer, Semiconductor Research Corporation, NIST Semiconductor Metrology R&D Workshop, April 2022

Advances and innovations in microelectronics will yield revolutionary new products but will require advanced metrology. The highly complex, integrated devices emerging for sophisticated future products present challenges for semiconductor manufacturing. Addressing the most critical of these challenges will help ensure that the U.S. leads global innovations and maintains a robust semiconductor industry.

Metrology is fundamental to microelectronics design, manufacturing, and packaging, as well as the critical materials and sub-strate supply chain. Physical and computational metrology are needed not only to aid in design, but also to assess, test, characterize, and inspect components during all phases of manufacturing. Metrology is required to identify, characterize, and mitigate defects and other issues that impact performance and quality and provides product assurance at many stages of manufacturing. Metrology is key for certifying materials at the beginning of manufacturing, as well as quality of the end products.

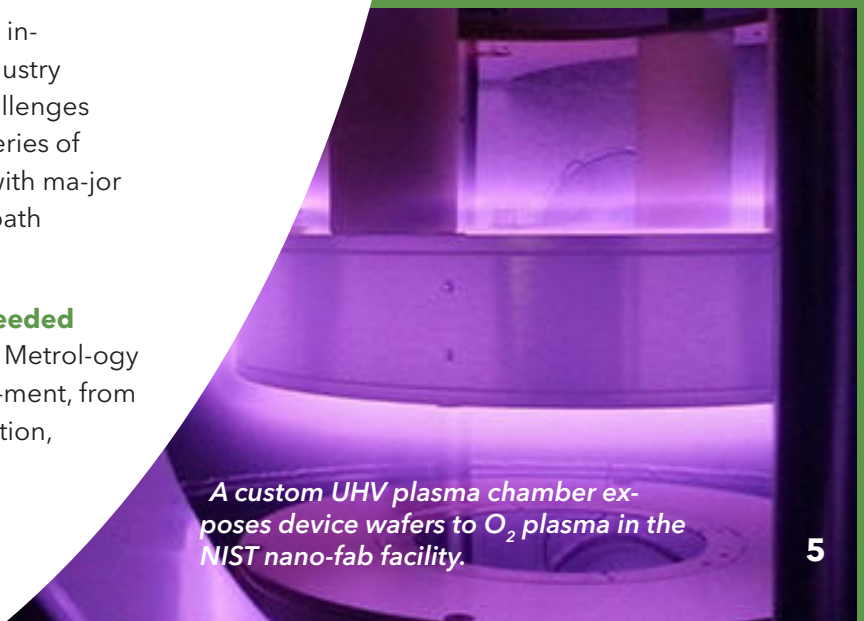
The requirements to characterize, test, and inspect next-generation devices, integrated circuits, and packaging are moving beyond the limits of today's measurement techniques. These complex devices require advanced nanoscale and subsurface measurement capabilities, including the ability to identify the type and position of atoms and assess buried layers. In some cases, metrology must also be suitable for in-line high-volume production, be non-destructive, and be able to provide results in real time.

Recognizing that metrology is critical to enabling future innovations in microelectronics, NIST has worked with industry stakeholders to identify the most pressing technical challenges requiring R&D. Information gained by NIST through a series of workshops, a request for information, and discussions with ma-jor companies has helped to inform a proposed strategic path forward focused on seven **Grand Challenges**.

The Grand Challenges outline the metrology R&D needed to strengthen the domestic semiconductor industry. Metrol-ogy is needed throughout all stages of technology develop-ment, from fundamental science through applied R&D, demon-stration, manufacturing, and deployment.

NIST is at the forefront of metrology for semiconductor manufacturing via industry partnerships.

NIST operates two nanofabrication facilities producing custom microfabricated devices for research and measurements to support electrical standards, quantum computing, and communications. Researchers also create custom devices for partner institutions to test new concepts. The facilities each house about 50 instruments that deposit very thin layers of materials on silicon wafers, transfer patterns to the wafers, and precisely and selectively subtract material to make custom nanoscale devices and structures.



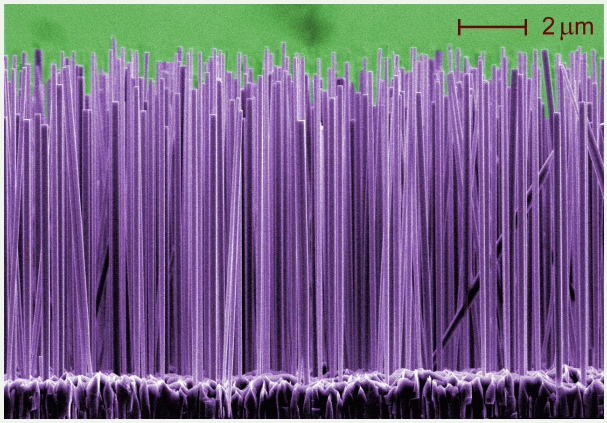
A custom UHV plasma chamber exposes device wafers to O_2 plasma in the NIST nano-fab facility.

Metrology for Materials Purity, Properties, and Provenance

MATERIALS ADVANCES IN MICROELECTRONICS

- **Metals to replace copper in ultrasmall interconnects–**Materials such as cobalt and ruthenium are being explored for tiny interconnects as scaling of devices continues to 3 nm and below, where layers must be very thin and conductive.
- **Dielectrics for 6G packaging–**Higher radio frequencies (several hundred gigahertz) require new types of dielectric materials. Materials must be temperature-resistant to withstand manufacturing processes and heat generation caused by signal loss in complex devices.
- **2D metal chalcogenides–**promising materials for broadband and high-performance photodetectors due to higher carrier mobility, absorption coefficient and narrow bandgap range.
- **Wide-bandgap semiconductors–**permit devices to operate at much higher voltages and temperatures than conventional semiconductor materials like silicon. Wide-bandgap semiconductors are the key component used for solid-state lighting, power electronics, and radio frequency (RF) applications, such as cell phones and radar.

NIST "grows" semiconductor nanowires that emit ultraviolet light as part of a project to make prototype nano-lasers and other devices and the measurement tools needed to characterize them.



New measurements and standards are needed to satisfy stringent requirements for the purity, physical properties, and provenance of materials.

Industry has seen explosive growth in both the diversity and global sourcing of materials for semiconductors over the past decade. As demand grows for faster, smaller integrated circuits, scientists have incorporated many new types of materials. Some companies report using hundreds of materials and chemicals during chip fabrication.

As devices become smaller, new paradigms in materials are required—new metals, dielectrics, etch gases, photoresists, antireflective coatings—and purity is of paramount importance. The properties and behavior of some of these materials are not well-characterized.

Supply sources for microelectronics materials have also become highly diversified and global. The market for semiconductor materials is enormous, reaching over $50 billion in 2018 and projected to be $70 billion by the end of 2025.[1] The introduction of new materials along with global sourcing has led to greater potential for contamination—and a need for consistency in purity, physical properties, and provenance of materials. Semiconductor fabricators need tools and metrology capability to verify the integrity of the materials being purchased. Materials can have multiple touchpoints along the chain of production, storage, transport, and delivery where contaminants can be generated or added.

1 *International Roadmap for Semiconductor Manufacture*. IEEE. 2020. https://irds.ieee.org/topics/semiconductor-materials

New measurements and standards are needed to ensure purity, physical properties, and provenance. Without these, atomic-scale defects or inadequate microscopic properties can severely limit yield, performance, and reliability of next-generation devices and integrated systems. Contamination control standards and the instrumentation to validate them, for example, would improve quality while reducing wafer defects—a large contributor to high costs and lower yields in semiconductor manufacturing.

Provenance *records the journey of a material from production to end use. The path can involve people (organizations, teams, individuals); locations (facilities, production lines within facilities, storage, equipment, warehouses, mines, barrels, etc.); and physical contact items (additives, solvents, gases, etc.). Provenance could record, for example, interactions with places and people who inspected the material, moved it, owned it, and stored it, along with its physical travels.*

Different materials manufacturers might not have the same accuracy in measurements or have unique methods for assessing if materials conform to quality or specifications. For example, semiconductor manufacturers want to be sure the dielectric properties of a material meet specifications—and may be uncertain about the accuracy of the supplier's methods. Some type of certification or accreditation, for example, would help assure manufacturers receiving materials of the provenance and consistency in the quality when purchased.

The challenge: Meet increasingly stringent requirements for semiconductor materials purity, physical properties, and provenance across a diverse supply chain through development of new measurements and standards.

The strategy: Develop measurement technologies, properties data, and standards focused on defect and contaminant identification. The objective is to support uniform materials quality across suppliers and to enable tracking of potential sources of impuri

The path forward: Conduct high-impact R&D and related activities in critical areas:

- New measurements with increased sensitivity and throughput for detection of particles and contaminants in materials throughout the supply chain, including in-lir quality assessment.
- Innovative, higher-throughput techniques for measuring physical properties for microelectronics feed materials.
- Evaluation and correlation of properties data across the materials supply infrastructu to support both standards and provenance.
- Standard Reference Materials (SRMs) for trace impurity detection and reference dat including those for thermophysical properties of materials.
- Documentary standards that can assist manufacturers in following materials through the supply chain, such as detailed versions of certificates of analysis (shows material properties, keeps track of any potential source of contamination).

Advanced Metrology for Future Microelectronics Manufacturing

THE LANGUAGE OF MICROELECTRONICS

- **DRAM and NAND**–high-volume, commodity memory semiconductor components that work together but have different functions. DRAM manages data and requires power (volatile); NAND flash stores data and requires no power (non-volatile).
- **Field-effect transistor (FET)**–a type of transistor that uses an electric field to control the flow of current in a semiconductor.
- **Manufacturing yield**–a quantitative measure of the quality of microelectronics processing. It is the fraction of product not discarded during manufacturing and packaging.
- **Transistor**–a semiconductor device used to amplify or switch electrical signals and power. The transistor is one of the basic building blocks of modern electronics.
- **3D transistor**–a transistor architecture formed vertically (three-dimensional) rather than horizontally (planar) for improved performance and increased density.

Breakthroughs in physical and computational metrology are needed for advanced manufacturing of future-generation devices.

The latest advances in microelectronics are incorporating more complex 3D devices and nanostructured materials. These multifaceted devices have many advantages, such as lower power consumption and smaller size.

Rapid growth of advanced node CMOS and other wafer-scale advanced devices and circuits (e.g., high frequency, silicon photonics) is expected in the future. CMOS scaling is increasingly focused on low voltage, cost-effectiveness, and higher performance. Advanced CMOS has gone from planar to 3D via integration techniques, and new transistor architectures have emerged, such as fin field-effect transistor (FinFET) and others. A promising approach for nanoscale transistors is the gate-all-around (GAA) FETs, in horizontal or vertical configurations, particularly for advanced nodes at 3 nm and beyond.

As devices become more complex, the metrology becomes more challenging. Measuring and characterizing structures is the traditional approach for identifying problem areas and ensuring yields in semiconductor manufacturing. However, when applied to 3D structures, metrology tools are more expensive and often exhibit significant gaps in capabilities.

Advanced node manufacturing is approaching the point where each atom's position and type within a 3D device needs to be known to meet the ever-increasing requirements for continued gains in system performance.

Part of the challenge is to characterize the inner or buried portions of 3D structures that comprise various materials/films, many layers and tiny channel holes—the more layers, the more difficult the metrology becomes. Further, no single metrology tool is able to make all the needed measurements. A suite of tools used for 2D characterization is often employed (e.g., electron microscopes, optical systems)—but these fall short in being able to penetrate layers adequately and at the small scale required. A concerted effort that combines R&D with standards development is needed to address this challenge.

The challenge: Ensure that critical metrology advances are made to keep pace with cutting-edge and future microelectronics and semiconductor manufacturing, while maintaining a competitive U.S. advantage.

The strategy: Develop advanced physical and computational metrology adaptable to next-generation manufacturing of advanced complex, integrated technologies and systems.

The path forward: Conduct activities in critical areas to develop innovative, cost-effective metrology applicable to 3D device and next-generation manufacturing, including tools and methods in the following critical areas:

- Properties of new materials and devices, such as GAA, complementary FET, and novel interconnects and dielectrics.
- Physical properties characterization (e.g., size, roughness, thermal, mechanical, electrical, magnetic, optical) for surfaces, buried features, interfaces, and devices with increased resolution, sensitivity, accuracy, and throughput.
- Rapid, high-resolution, non-destructive techniques for characterizing defects and impurities and correlating them with performance and reliability.
- Evaluation and correlation of relevant data across the semiconductor manufacturing process.
- Standards for process design, development, and control, such as reference materials and documentary standards.
- Statistical analysis for rare but catastrophic defects such as stochastic events in extreme ultraviolet (EUV) lithography.

Enabling Metrology for Integrating Components in Advanced Packaging

ADVANCED PACKAGING CONCEPTS

- **Heterogeneous integration–**refers to the integration of separately manufactured components into a higher-level assembly that, in the aggregate, provides enhanced functionality and improved operating characteristics.
- **Multi-chip modules–**multiple integrated circuits (ICs)/dies integrated into a single package or module to reduce required board space.
- **3D integrated circuit–**an IC formed by stacking wafers and/or dies vertically (three-dimensional) and connecting them electrically using through-silicon vias (TSVs).
- **System-in-package–**method to bundle multiple ICs in a single package, compared to system on chip (SoC) where functions on chips are integrated in the same substrate.
- **Fan-out wafer packaging–**package where connections are fanned out of the chip surface to enable more external inputs/outputs; uses epoxy mold compound to embed the die instead of placement on a substrate.
- **Integrated photonics–**an emerging branch of photonics in which waveguides and devices are fabricated as an integrated structure onto the surface of a flat substrate, or flat surface.
- **Optical interconnects–**refers to transmission of signals from one part of an integrated circuit or system to another using light.
- **Known good die–**chips that have been fully charaterized before being placed into their packages.

New metrology will enable complex integration of sophisticated components and novel materials for advanced microelectronics packaging.

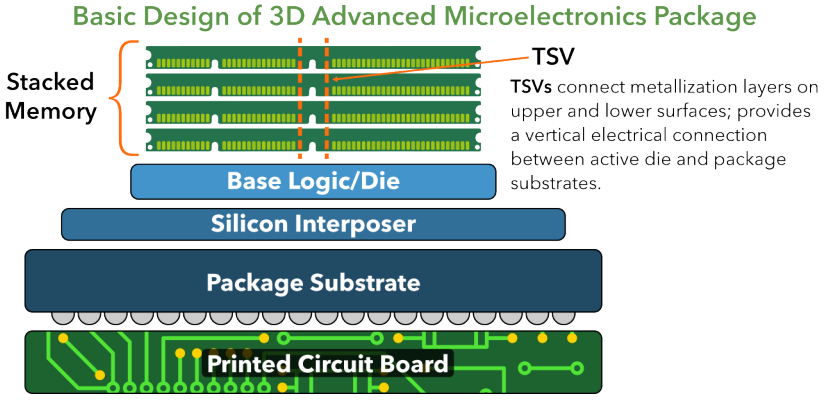
Advanced packaging has emerged as a critical element for continued performance gains in microelectronics. Advanced packaging enables a multitude of devices with different functions (logic, memory, GPS, power, accelerometers, etc.) to be integrated and packaged together to meet application-specific requirements. While improvements inside the chip have been used for decades to increase functionality, advances in packaging have emerged as an innovative, cost-effective approach.

Increasingly, consumers are seeking higher-performing and multi-functional devices that exhibit greater speed but are smaller and cost less; advanced packaging is an effective way to achieve these features. Significant improvements in system performance are obtained through the co-design and integration of disparate components within the package.

The combination of components will vary depending on the advanced function desired and can include multiple dies integrated in the same package (smaller footprint). Packaging pulls all the components together, resulting in a more powerful, higher-performing heterogeneous system and potentially reducing time to market. Heterogeneous integration is an enabling approach and critically important to future devices where higher performance, smaller and lighter form, lower power requirements, and lower cost are essential.

Integration of different materials and components requires new measurement standards and capabilities that span multiple length scales and physical properties with validated accuracy to ensure high yield and performance.

The processes and techniques used to create advanced packaging occur post-fabrication and impact both metrology and inspection. Materials may not be standard, or packages may use different types of materials, impacting inspection requirements. Advanced packaging also presents unique measurements for back end processes and technologies, such as measurement of bump spacing and dimensions and detection and characterization of buried defects. These rapidly emerging advanced packaging concepts will require flexible, adaptable measurement systems for controlling various parameters (both 2D and 3D).



Advanced packaging allows multiple systems and materials–such as basic logic, memory, and RF communications (Next G, WiFi, Bluetooth)–to be incorporated in one package.

The challenge: Provide enabling metrology that spans multiple length scales and physical properties and supports acceleration of advanced packaging concepts for future-generation microelectronics.

The strategy: Develop metrology to enable complex integration of sophisticated components and novel materials for advanced microelectronics, strengthening the domestic semiconductor packaging industry and U.S. leadership in this critical sector.

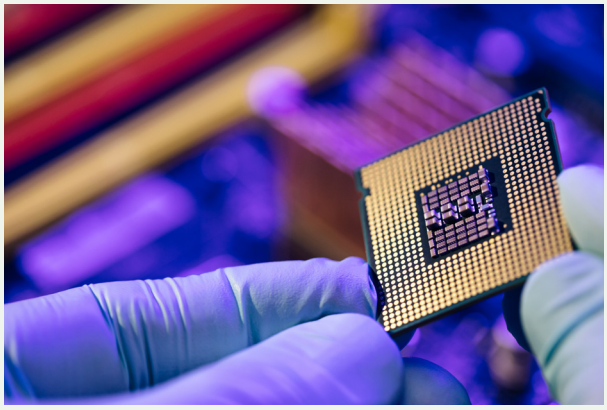
The path forward: Conduct R&D to develop metrology to address the unique challenges presented by advanced packaging, including subsurface features and aspects related to heterogeneous integration and other innovative concepts. Critical areas include:

- Measurements for in situ, rapid measurements and verification methods for interfaces and subsurface interconnects, and internal 3D structures including warpage, voids, substrate yield, stresses, adhesion, and reliability with improved throughput and resolution.
- Physical properties (e.g., size, thermal, mechanical, electrical, magnetic, optical) for films, surfaces, buried features, and interfaces.
- Methods for integrating chiplets, dielets, SoCs, and memories into packages.
- Mechanical measurements for component integration (e.g., hybrid bonding and interfacial adhesion and bond integrity).
- Evaluation and correlation of data across the packaging process.
- Standards for packaging, such as reference materials and documentary standards for areas including chiplets and SoCs.

Modeling and Simulating Semiconductor Materials, Designs, and Components

"We need to invest in modeling and electronic design automation for reduced costs and increased throughputs… …government investment is critical for U.S. semiconductor manufacturing capabilities."

Bill Deal, Consulting Engineer, Northrop Grumman, NIST Semiconductor Manufacturing Metrology Workshop, April 2022



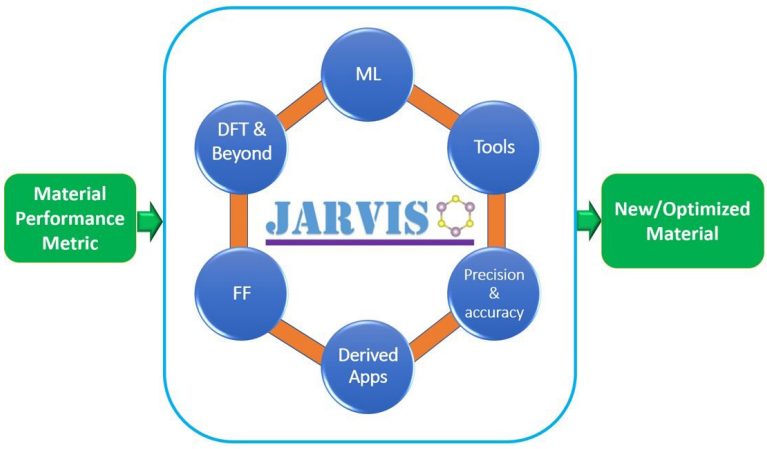
Microprocessor with visible silicon core and cache chip.

Advanced metrology tools are needed for effectively modeling and simulating next-generation semiconductor materials, processes, devices, circuits, and system designs.

Hardware design is becoming more complex and multi-disciplinary, involving software, manufacturing, and new materials. Modeling and simulation are key elements used by the semiconductor industry to decrease the development time required to get new technologies to market. New models are continuously emerging as requirements for faster compact circuits and systems become more stringent. Models and simulations must analyze sophisticated device features and perform rigorous testing and optimization under a variety of environmental and operating conditions.

Physics-based models are intended to enable selection of optimal device features and performance when operating in a variety of conditions. While these models are relatively accurate, the calculations may not be fast enough for higher-level analysis, including circuit design. In that case, empirical models (computer-based models based on experimental data) are applied. The result is a trade-off between the accuracy of the device model and computational speed.

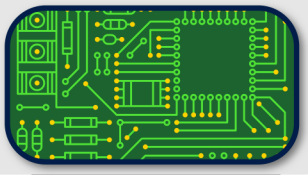
With more complex and future technologies, systems are pushed to operate at higher frequencies, resulting in higher packaging density and disparate components. With these devices, designers need to focus more on effects such as electromagnetic coupling between circuits or thermal issues due to greater component density. Electrical performance may degrade as speed and density increase, resulting in the need to model and control signal, power, and thermal integrity. Smaller and higher-frequency device profiles require greater accuracy of dopant and stress profiles, as well as other parameters that are important during manufacturing. The greater the number of interacting components, the larger the issue becomes. Simulators for future designs must have the capability to model multiple physical effects in large heterogeneously integrated systems.



JARVIS is a repository for standardizing computational tools for materials modeling including force fields (FF) and ML for density functional theory (DFT). JARVIS has over 6,000 users and 300,000 downloads. For more information: jarvis.nist.gov

Significant improvements in model characterization methods, data handling, and verification are needed across the semiconductor value chain to maximize their effect.

The challenge: Improve the tools needed to effectively model and simulate future semiconductor materials, processes, devices, circuits, and microelectronic system designs.



The strategy: Develop advanced design simulators based on multi-physics models, a spectrum of critical measurements, and next-generation concepts such as artificial intelligence, creating a suite of tools to empower U.S. microelectronics designers.

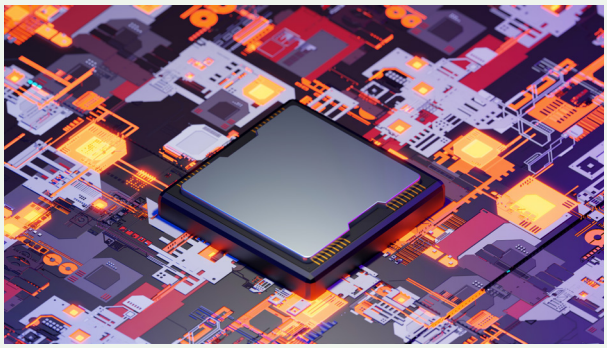
The path forward: Conduct R&D to develop robust data, mathematical models, and measurement techniques for important future device parameters that are needed to support effective design simulators. Critical R&D areas include:

- Multi-physics models, including those that capture thermal, chemical, physical, mechanical, signal integrity, reliability, power consumption, and other parameters.
- Measurements of material, component, and circuit properties across a broad temperature, bias, and frequency range as input to, and as verification of, the above models.
- Application and validation of advanced analytics such as ML and AI for modeling and optimization of complex materials, circuits, and systems operating in real environments.
- Methods for robustly estimating model uncertainty.

Modeling and Simulating Semiconductor Manufacturing Processes

"When conflicts and disturbances occur in physical space, virtual models can be tested in real time, predict future events, feed the information back to the physical space, identify where to improve the design, and provide efficient communications between customers and designers."

Dr. John Allgair, Program Technical Vice President, BRIDG



A digital twin virtually represents a device or process across its lifecycle; relies on simulation, ML, and AI to make decisions; and is updated continuously with real-time data. Digital twins enable manufacturers to reproduce and model an entire process, enhancing quality, reliability, productivity, and trust and assurance.

Breakthroughs are needed to enable tools to seamlessly model and simulate the entire semiconductor manufacturing process.

Modeling and simulation are critical to the manufacturing of microelectronics and semiconductors, from materials inputs to wafer fabrication and system assembly. Effective modeling of manufacturing processes enables better control of essential performance parameters, identification of flaws, defects and their root causes, quality assurance, and predictive equipment maintenance.

Semiconductor manufacturing can have literally thousands of steps, as chips with multiple layers, components, and systems are integrated and assembled into complex architectures. Metrology plays a key role in every step of manufacturing, and computational metrology (models built on data) can be especially critical.

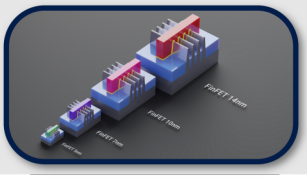
Breakthroughs in measurements and development of consensus standards are critical to improvements in data handling, analytics, virtualization, and automation to enable greater efficiency in manufacturing and accelerated time to market. Inadequate manufacturing process models and metrology can contribute significantly to poor yields, resulting in fewer chips and systems that are viable for integration into end products and delaying overall production.

While simple physical models are commonly applied due to their faster computation times, these do not meet the demands of more complex and sophisticated manufacturing processes. Models that can can accurately simulate next-generation device manufacturing parameters and processes are needed.

Digital twins are one approach that shows great promise. For example, a robust virtual twin of a fabrication facility could model the operation of each piece of equipment and all related operations. This enables optimization of manufacturing processes and parameters to improve yield and reliability. For maintenance, a virtual twin could provide feedback about potential equipment failures or preventive maintenance scheduling, enabling technicians to make repairs before equipment breaks down.

Massive amounts of disaggregated or poorly utilized data (as much as 15 TB/day/fab) are created and collected daily throughout the semiconductor value chain. Significant breakthroughs are needed to enable tools to seamlessly model and simulate the entire semiconductor manufacturing process and effectively utilize (and make decisions upon) these large, disparate data sets.

The challenge: Seamlessly model and simulate the entire semiconductor value chain, from materials inputs to chip fabrication, system assembly, and end products.

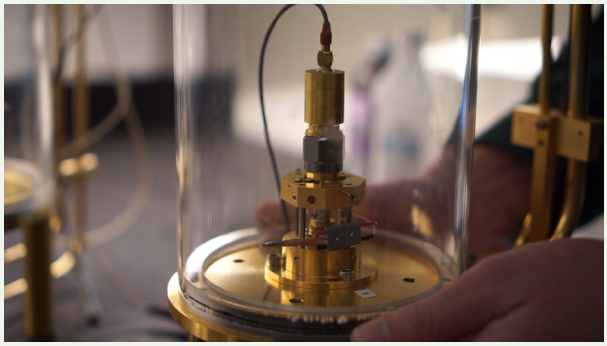


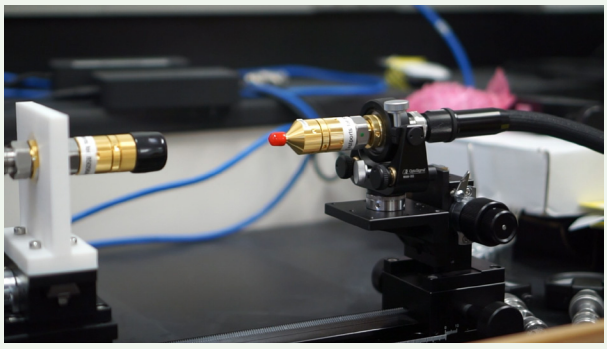
The strategy: Create a suite of advanced computational models, methods, data, standards, and tools that will enable domestic semiconductor manufacturers and the value chain to improve overall yields, accelerate time to market of devices, and enhance competitiveness in global markets.

The path forward: Conduct R&D to develop a variety of effective manufacturing simulation tools and related standards that can be applied to in-line processes and model key parameters. Critical R&D areas include:

- Modeling, data analysis, and validation tools to enable efficient process development and optimization.
- Standards, protocols, and standard data for automation and virtualization.
- Measurements and standards supporting digital twins, from individual processing steps up to the complete chip fabrication and system assembly.
- Application and validation of advanced analytics such as ML and AI for modeling and optimization of complex manufacturing process design, development, automation, and integration.

Standardizing New Materials, Processes, and Equipment for Microelectronics





NIST maintains the U.S. National Standards for RF quantities, including power, scattering parameters, thermal noise, antenna gain, and the Josephson Volt. Calibrated electrical measurements, traceable to the SI, are critical for all aspects of microelectronics from the characterization of components and design of circuits through production test.

Photos courtesy of NIST

New standards and validation methods are needed to accelerate the development of future information and communication technologies.

Standards provide technical specifications, performance criteria, and other requirements to guide the design and production of materials, processes, and equipment. Manufacturing to a standard enables compatibility and interoperability across the supply chain and ensures product performance, quality, reliability, safety, and security. The use of standards can even drive industry innovation, cost reduction, and holistic solutions.

As new materials and highly integrated microelectronics products emerge, standardization is critical to ensuring the continued growth of the domestic semiconductor industry. In 1973, the proliferation of over 2,000 semiconductor wafer specifications led to major inefficiencies. Faced with these barriers, wafer manufacturers collaborated to develop consensus wafer specifications, and within a few years, over 80% of wafers conformed to the newly developed standards. Establishing consistency in wafer size allowed equipment companies to focus on product differentiation and innovations that improved performance and lowered costs.[2]

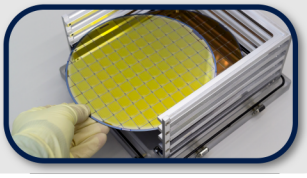
2 *The Semiconductor Industry's Secret to Success. Semiconductor Equipment and Materials International (SEMI).* August 12, 2019. https://www.semi.org/en/blogs/technology-trends/the-semiconductor-industrys-secret-to-success

Today, the integration of new materials, processes, and equipment for both front- and back-end semiconductor manufacturing calls for a modernized set of standards to improve accuracy, traceability, validation, and the security of critical microelectronic systems. Standards cover a broad spectrum and include SRMs, SRD, equipment calibration standards, and written protocols and guidelines.

Verification and validation (V&V) refers to independently testing that a product or system meets its specifications and intended purpose. In manufacturing, V&V takes data from process design through production to scientifically demonstrate that the process or device consistently delivers as intended.

NIST staff using EUV reflectometer at NIST's SURF-III synchrotron facility to calibrate specialized optics for EUV lithography systems.

The challenge: Create the standards and validation methods necessary to accelerate the development and manufacturing of future information and communication technologies.



The strategy: Create standards and validation protocols to support the use of new materials, processes, and equipment in future-generation microelectronics, paving the way for accelerated innovation and cost-competitiveness in U.S. industry.

The path forward: Conduct R&D, data collection, process validation, and other standards-related activities to support the development of documentary standards, SRMs, and calibration protocols and services for next-generation semiconductor manufacturing. Critical areas of pursuit include:

- SMRs, data, instruments, and calibration and measurement services; product development kits; and a diversity of best-known methods.
  - Reference materials to detect defects, contaminants, and trace impurities at the nanoscale.
  - Reference materials for nanoscale dimensional and materials characterization.
  - Calibration, validation, and new methods to enable high-accuracy fleet matching for equipment in both process development and high-volume manufacturing (i.e., matching the suite of tools to the process/materials of use).
  - SMRs and data for advanced packaging and heterogeneous integration, including high-frequency electrical properties and thermomechanical properties.
- Standards for interoperable equipment and software from different vendors that ensure the protection of intellectual property (IP), data integrity, and provenance across the supply chain.
- Standards for tracking materials from creation to end use in the fab, including anything that could alter the properties of the material.

Metrology to Enhance Security and Provenance of Microelectronic-based Components and Products

"Security begins before chip design even starts…"

"There is a critical need for a structured and uniform approach to security across the manufacturing lifecycle…"

Matthew Areno, Senior Director of Security Assurance and Cryptography, Intel, NIST Semiconductor Metrology R&D Workshop, April 2022

Advances in metrology are needed to enhance the security and provenance of microelectronic components and products across supply chains and to improve trust and assurance.

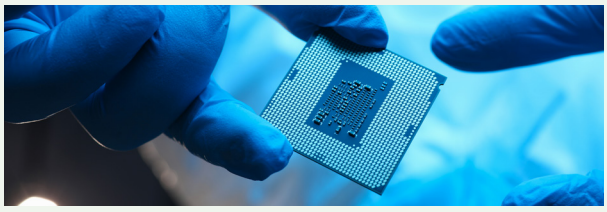
Securing the tiny, intricate semiconductor chips essential to many electronic systems can be challenging. The increasing complexity involved in the development, integration, and post-deployment use of microelectronics presents new security risks and vulnerabilities. Microelectronics manufacturing has a complicated global supply chain with production and use across multiple continents. Systems in which safety and reliability are critical—defense, aviation, automobiles, medical devices, telecommunication, the electric grid—are especially vulnerable.

Recent chip shortages have exacerbated counterfeiting, IP theft, the reverse engineering of designs, and the production of low-quality and defective chips. Without the means of verifying the provenance of the semiconductor, malicious circuits could be added anywhere along the supply chain, allowing bad actors to bypass defense mechanisms, disrupt devices, and steal user information. Robust hardware security has become a requirement rather than a feature.

To meet these challenges, the U.S. Department of Defense is adopting "zero trust" policies, meaning that microelectronics can be considered safe only once they are validated. Trust and assurance is also required by the private sector to ensure resiliency of essential markets and

TRACKING CHIPS THROUGHOUT THE SUPPLY CHAIN

Suppliers to the U.S. Department of Defense must comply with strict requirements for defense and critical infrastructure through the Rapid Assured Microelectronics Prototypes (RAMP) using Advanced Commercial Capabilities Project. RAMP provides a secure, scalable platform for microelectronics design, manufacturing, and supply chain management. A coalition of industry leaders are building capabilities to support RAMP including Microsoft, Applied Materials, Inc., BAE Systems, Battelle Memorial Institute, Cadence Design Systems, GlobalFoundries, Intel Corporation, Nimbis Services, Inc., Northrop Grumman, Siemens EDA, Synopsys, Inc., and Zero ASIC Corporation.



infrastructure, such as the financial market, electric grid, healthcare system, transportation, and communications. Advanced imaging technologies, forensics, and other methods are being used to detect counterfeits and malicious circuits. Semiconductor components are being authenticated via markings and tags to track supply chain movements and provide provenance of the product.

However, the challenge of hardware security protection goes across the supply chain, covering manufacturers and material suppliers, as well as a wide spectrum of commercial sectors. The Nation's reliance on microelectronics for so many critical technologies requires a comprehensive, robust approach to hardware security.

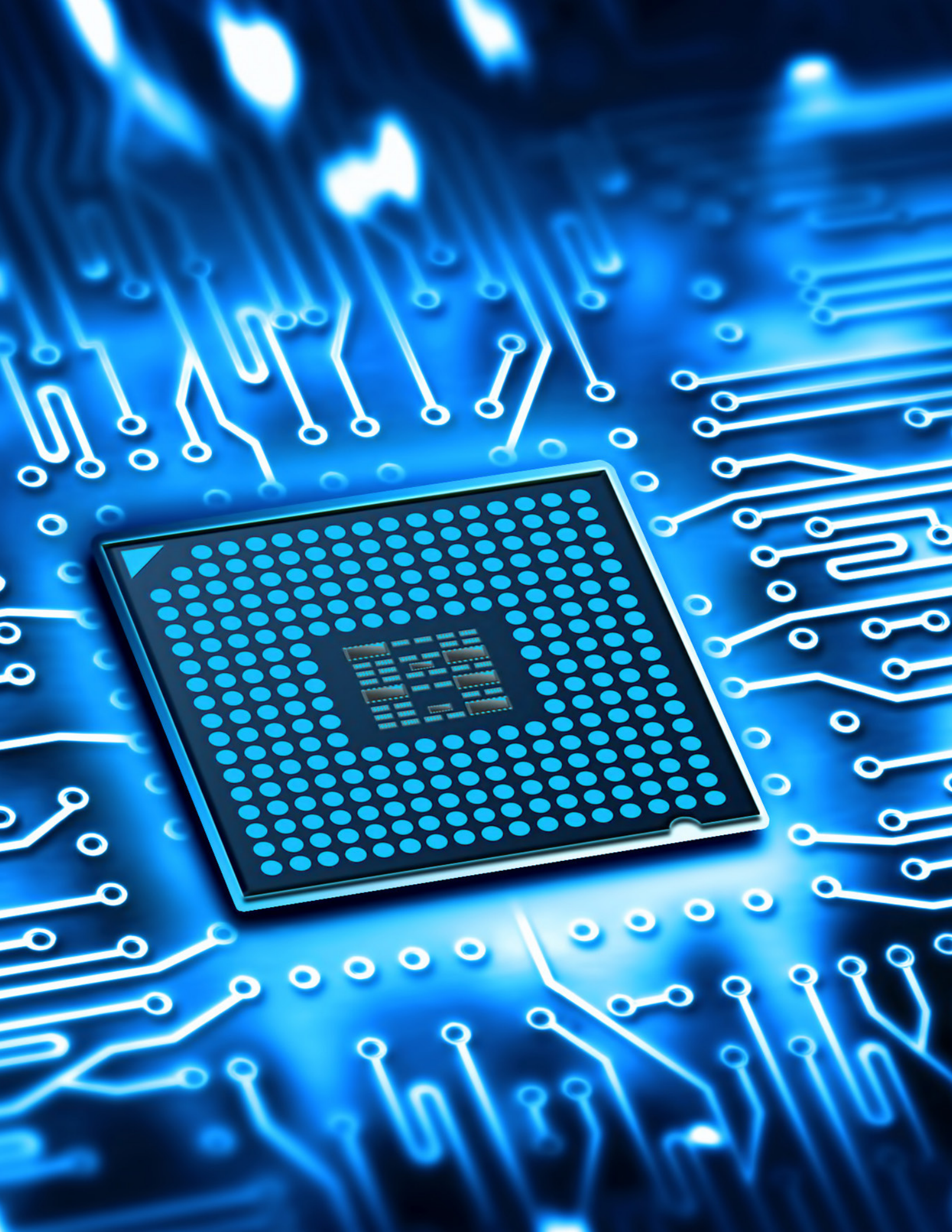
Many aspects of security must be considered to create protected hardware environments. For example, integrated chiplets could have embedded malware, and assembled parts could have compromised components. New methods and standards are needed to create a semiconductor ecosystem that is rooted in trust and assurance, from input materials to the finished products where systems are coupled and integrated. The approach includes standards and guidelines for security analytics, combined with a broad vulnerability strategy for testing and verification throughout the product life cycle.

The challenge: Create the metrology advances needed to enhance the security and provenance of microelectronic components and products across supply chains and increase trust and assurance.

The strategy: Pursue a comprehensive approach to hardware security protection that includes standards, protocols, formal testing processes, and advanced computational technologies while providing avenues for assurance and provenance of microelectronic components across the supply chain and end products.

The path forward: Conduct activities to support the development of standards, protocols, and testing processes for analyzing security vulnerabilities in microelectronics across their entire life cycle. Critical areas of pursuit include:

- Methods, reference design kits, and guidelines for security analytics and automation, including pervasive security to address formalized threat models.
- Enhanced vulnerability management across the overall product life cycle from inception to end of life, including activities such as:
  - Formal testing and processes for independent V&V.
  - Tracking of materials and components, as well as detecting and mitigating trigger mechanisms.
  - Common test structures, test methods, and test and measurement strategies for end-to-end provenance.
- Documentary standards for hardware security and provenance.
- Development and use of trusted emerging techniques, e.g., AI and ML methods across the entire semiconductor value chain.



Path Forward

Semiconductors are critical to our Nation's economic growth, national security, and public health and safety. Revolutionary advances in semiconductors continue to drive innovation in communications, information technology, health care, military systems, transportation, energy, and infrastructure. The potential for semiconductors to create transformational change is multiplying as they become smaller, faster, and more sophisticated, delivering unprecedented performance.

Metrology plays a key role in semiconductor manufacturing. As devices become more complex, smaller, and multi-layered, the ability to measure, monitor, predict, and ensure quality in manufacturing becomes much more difficult and uncertain. Today, the domestic semiconductor industry faces some of these metrology challenges with workarounds and inadequate tools, limiting production yields, impacting quality, and increasing costs. As greater demands are put on semiconductor device performance and material requirements, these challenges will continue to intensify. The metrology challenges impacting the U.S. semiconductor industry are at a critical stage and urgently need to be addressed.

Addressing metrology challenges now will strengthen the Nation's semiconductor industry.

This report has outlined the metrology grand challenges facing the rapidly changing semiconductor sector. Addressing these challenges now will create a stronger domestic industry and help position the United States as a global leader in metrology essential for next-generation microelectronics. There are many high-impact outcomes to be gained, specifically by:

- *Advancing **U.S. leadership in documentary standards development** to strengthen U.S. global competitiveness in advanced microelectronics materials, design, manufacturing, and packaging.*
- *Developing and deploying **critically needed measurement services** (reference materials, reference data, calibrations) to drive U.S. leadership in microelectronics manufacturing and related technologies.*
- *Developing and deploying **innovative manufacturing metrologies** to enable U.S. industry to increase manufacturing yield, improve performance, and accelerate time to market for next-generation microelectronics.*

"We're going to construct an entire semiconductor ecosystem right here in the United States of America."

Commerce Secretary Gina Raimondo, August 9, 2022

Modern high-tech robot arm holding chip for contemporary supercomputer processor.

"**We can't improve what we don't measure.**"

"We must lead in **both technology and workforce development** to emerge as true front-runners."

Todd Younkin, Semiconductor Research Corporation, speaking on the 2030 Decadal Plan for Semiconductors at the NIST Semiconductor Manufacturing Metrology R&D Workshop, April 2022

NIST is working with the semiconductor industry to overcome the approaching physical limitations to chip improvement. NIST partnered with semiconductor companies through the Nanoelectronics Research Initiative (NRI) to identify and tackle the biggest research challenges facing the industry. More than 700 students trained for high-tech professions through the NRI, and 60 patent applications were filed based on the work leveraging NRI.

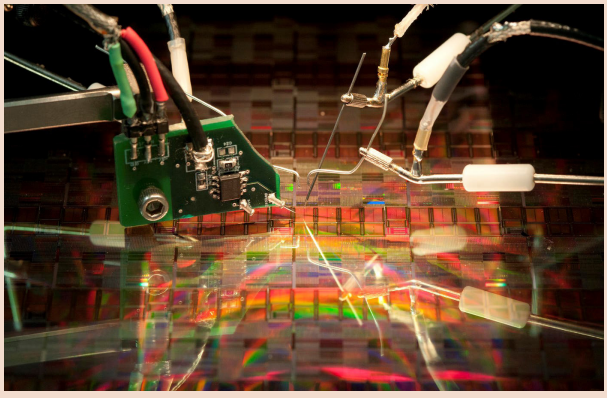


Photo of a high-speed, amplified probe tip used to collect reliability data in the NIST Advanced Device Characterization and Reliability laboratory.

Credit: Photo by Erik Secula

- *Developing and deploying **novel assurance and provenance technologies** to reduce microelectronics security risks across supply chains, from design and development to manufacturing, packaging, and end of life.*
- *Establishing **advanced metrology R&D testbeds** with state-of-the-art equipment and tools to drive measurement science innovations for next-generation microelectronics.*
- *Building and sustaining **collaborative partnerships with industry** to accelerate the transfer of technology from the laboratory to the commercial marketplace and support talent development and deployment.*

Metrology advances are foundational to accelerating innovations in the semiconductor industry. As the U.S. national measurement institute, NIST has a key role to play in the development of enabling metrology tools, standards, and methods for semiconductor manufacturing.

This report is an important roadmap for NIST to establish and expand metrology R&D programs to support the strategic priorities of the U.S. semiconductor industry for next-generation microelectronics. This strategic approach is aligned with NIST's mission: *to promote U.S. innovation and industrial competitiveness by advancing measurement science, standards, and technology in ways that enhance economic security and improve our quality of life.*

Through the CHIPS Act, the U.S. government has authorized incentives and programs to support U.S. semiconductor manufacturing, R&D, and supply chain security. Congress has explicitly authorized and appropriated funding to accelerate metrology R&D for next-generation microlectronics at NIST to achieve the objectives of the legislation. NIST will work synergistically and in close coordination with the other CHIPS Act programs, i.e., Incentives, National Semiconductor Technology Center, National Advanced Packaging Manufacturing Program, and Manufacturing USA Institute(s).

Acknowledgements

This strategic report was prepared through the collaborative insights of semiconductor stakeholders from industry, academia, and government who presented information at two well-attended NIST-hosted workshops in April 2022 (acknowledged below). We also appreciate contributions from the over 800 workshop participants, including NIST technical experts, and those who responded to a Federal Request for Information. Additional thanks go to Energetics for preparation of this report.

INDUSTRY

Ofer Adan, Applied Materials
John Allgair, BRIDG
Andy Antonelli, Onto Innovation, Inc.
Matthew Areno, Intel Corporation
Norman Chang, ANSYS
William Deal, Northrop Grumman Space Systems
Chris Deeb, Intel Corporation
Regina Feed, Applied Materials
Nelson Felix, IBM
Laurie Giandomenico, MITRE
Michael J. Hill, Intel Corporation
Gerard John, Amkor Technology, Inc.
Matt Kelly, IPC
Deepak Kulkarni, AMD
Raj Kumar, TTM Technologies
Roya Lahiji, Intel Corporation
Dale Lee, Plexus Corporation
Serge Leef, Microsoft
Qinghuang Lin, Lam Research
Pilin Liu, Intel Corporation
Dale McHerron, IBM Research
Victor Moroz, Synopsys
Rama Puligadda, Brewer Science
Marc Swinnen, ANSYS
Zhengquan Tan, KLA
Stuart Tison, Entegris
Bill Tonti, IEEE
Alok Vaid, GlobalFoundries
E. Jan Vardaman, TechSearch International, Inc.
Ganesh Vijayaraghaven, Air Products
Todd Younkin, Semiconductor Research Corporation

ACADEMIA

Peter Aaen, Colorado School of Mines
Suman Datta, University of Notre Dame
Alain Diebold, State University of New York (SUNY) Polytechnic Institute
Bongtae Han, University of Maryland
Carol Handwerker, Purdue University
Amy Marconnet, Purdue University
Michael Shröter, Technical University of Dresden
Mark Tehranipoor, University of Florida

GOVERNMENT

National Institute of Standards and Technology, U.S. Department of Commerce (Organizers/Authors)

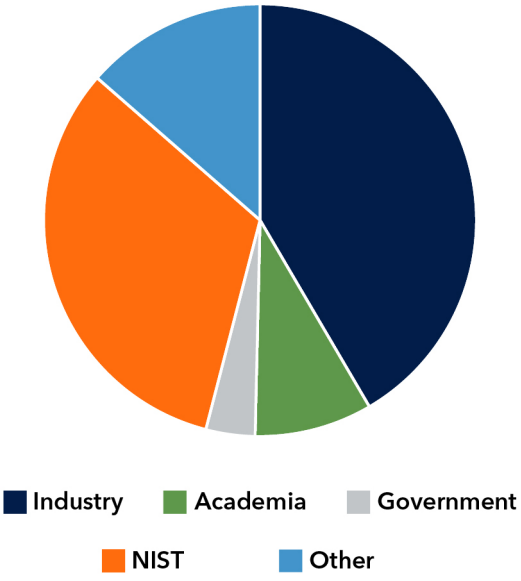
Anita Balachanhdra
David Gundlach
Paul D. Hale
Kevin K. Jurrens
R. Joseph Kline
Timothy McBride
Ndubuisi George Orji
Sanjay (Jay) Rekhi
David G. Seiler
Sivaraj Shyam-Sunder

Stakeholder Engagement

NIST conducted Semiconductor Manufacturing Metrology R&D Workshops on April 6–7 and 20–21, 2022, to gather insights from stakeholders on the important metrology needs for manufacturing. Both events included full-day plenary and roundtable panel discussions, followed by breakout sessions guided by professional facilitators.

The workshops were attended by over 800 stakeholders and experts from the semiconductor and microelectronics community, including representatives from industry, government, academia, and private research institutions. Over 50% of attendees represented private companies, trade associations, research institutes, and universities involved in the semiconductor manufacturing supply chain and related research.

Participating stakeholders encompassed a wide range of semiconductor interests and expertise across the supply chain, including design, materials, manufacturing processing and equipment, packaging, and security.



Distribution of Semiconductor Manufacturing Metrology R&D Workshop attendees.

The information gained through the workshops and extensive stakeholder engagement was instrumental in identifying the critical metrology challenges that must be addressed for next-generation microelectronics and provided a foundation for this report on strategic opportunities.

Acronyms

2D	Two-Dimensional
3D	Three-Dimensional
AI	Artificial Intelligence
CHIPS Act	Creating Helpful Incentives to Produce Semiconductors for America Act
CMOS	Complementary Metal–Oxide–Semiconductor
Cu	Copper
DFT	Density Functional Theory
DRAM	Dynamic Random Access Memory
EUV	Extreme Ultraviolet
FET	Field-Effect Transistor
FF	Force Fields
GAA	Gate All Around
GHz	Gigaherz
GPS	Global Positioning System
IC	Integrated Circuit
IP	Intellectual Property
ML	Machine Learning
NRI	Nanoelectronics Research Initiative
NDAA	William M. Thornberry National Defense Authorization Act
NAND	Most common type of flash memory
NIST	National Institute of Standards and Technology
nm	Nanometer(s)
OEM	Original Equipment Manufacturer
R&D	Research and Development
RAMP	Rapid Assured Microelectronics Prototypes
RF	Radio Frequency
SI	International System of Units
SIP	System-in-Package
SoC	System on Chip
SRD	Standard Reference Data
SRI	Standard Reference Instrument
SRM	Standard Reference Material
TB	Terabyte
TSV	Through-Silicon Via
V&V	Verification and Validation

PHOTOS
(unless already credited)

front/back cover main	AdobeStock 297362425
(from top) front cover inset 1	AdobeStock 201891922
front cover inset 2	AdobeStock 206119643
front cover inset 3	AdobeStock 283992784
front cover inset 4	iStock Photo 000016963250
page 1	AdobeStock 123424452
page 4	iStock Photo 000014939237
page 5	National Institute of Standards and Technology
page 6	National Institute of Standards and Technology
page 8	Lam Research Corporation
page 9	AdobeStock 240748820
page 12	AdobeStock 405124231
page 14	AdobeStock 473628150
page 17	National Institute of Standards and Technology
page 18	AdobeStock 352217571
page 20	AdobeStock 51490712
page 21	AdobeStock 289023550

FOR MORE INFORMATION

www.nist.gov/semiconductors

chips@nist.gov

NIST | NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

www.doi.org/10.6028/NIST.CHIPS.1000